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JC872 U.S. PTO 09/811915 03/19/01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
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VN		"WAFER LEVEL TEST AND BURN IN", IBM Technical Disclosure Bulletin, January 1992, pp. 401-404;
VN		"MULTI-LAYER CERAMIC SPACE TRANSFORMER FOR WAFER LEVEL STRESS", IBM Technical Disclosure Bulletin, April 1999, pp. 385 - 386;
VN		"WAFER BURN-IN ISOLATION CIRCUIT", IBM Technical Disclosure Bulletin, November 1989, pp. 442-443

EXAMINER Minh Nguyen DATE CONSIDERED 11/21/2002

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.